Electronics & Communication Engineering

#### Digital Electronics –II

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#### **Chapter-5, Sequential Circuits Synchronous Sequential Logic**

Every digital system is likely to have combinational circuits, most systems encountered in practice also include storage elements, which require that the system be described in term of sequential logic.



Fig. 5-1 Block Diagram of Sequential Circuit

## Synchronous Clocked Sequential Circuit

A sequential circuit may use many flip-flops to store as many bits as necessary. The outputs can come either from the combinational circuit or from the flip-flops or both.



Fig. 5-2 Synchronous Clocked Sequential Circuit



#### **SR Latch**

The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates. It has two inputs labeled S for set and R for reset.



Fig. 5-3 SR Latch with NOR Gates

#### **SR Latch with NAND Gates**



(a) Logic diagram

(b) Function table

Fig. 5-4 SR Latch with NAND Gates

#### **SR Latch with Control Input**

The operation of the basic SR latch can be modified by providing an additional control input that determines when the state of the latch can be changed. In Fig. 5-5, it consists of the basic SR latch and two additional NAND gates.



(a) Logic diagram

(b) Function table

Fig. 5-5 SR Latch with Control Input



One way to eliminate the undesirable condition of the indeterminate state in SR latch is to ensure that inputs S and R are never equal to 1 at the same time in Fig 5-5. This is done in the D latch.



Fig. 5-6 D Latch

## **Graphic Symbols for latches**

A latch is designated by a rectangular block with inputs on the left and outputs on the right. One output designates the normal output, and the other designates the complement output.



SR

Fig. 5-7 Graphic Symbols for Latches

D



The state of a latch or flip-flop is switched by a change in the control input. This momentary change is called a trigger and the transition it cause is said to trigger the flip-flop. The D latch with pulses in its control input is essentially a flip-flop that is triggered every time the pulse goes to the logic 1 level. As long as the pulse input remains in the level, any changes in the data input will change the output and the state of the latch.



In Fig (a) a positive level response in the control input allows changes, in the output when the D input changes while the clock pulse stays at logic 1.



(a) Response to positive level



(c) Negative-edge response

## **Edge-Triggered D Flip-Flop**

The first latch is called the master and the second the slave. The circuit samples the D input and changes its output Q only at the negative-edge of the controlling clock.



#### **D-Type Positive-Edge-Triggered Flip-Flop**

Another more efficient construction of an edge-triggered D flip-flop uses three SR latches. Two latches respond to the external D(data) and CLK(clock) inputs. The third latch provides the outputs for the flip-flop.



Fig. 5-10 D-Type Positive-Edge-Triggered Flip-Flop

#### **Graphic Symbol for Edge-Triggered D Flip-Flop**



(a) Positive-edge (a) Negative-edge

Fig. 5-11 Graphic Symbol for Edge-Triggered D Flip-Flop





There are three operations that can be performed with a flip-flop: set it to 1, reset it to 0, or complement its output. The JK flip-flop performs all three operations. The circuit diagram of a JK flip-flop constructed with a D flip-flop and gates.



(a) Circuit diagram



The J input sets the flip-flop to 1, the K input resets it to 0, and when both inputs are enabled, the output is complemented. This can be verified by investigating the circuit applied to the D input:

D = JQ' + K'Q



(b) Graphic symbol

JK F	lip-F	lop	inola sull to inc
JI	K	Q(t+1)	entrans the trip.
0 (	0	Q(t)	No change
0	1	0	Reset
1 (	0	l lo one of F	Set
1	1 25	Q'(t)	Complement



The T(toggle) flip-flop is a complementing flip-flop and can be obtained from a JK flip-flop when inputs J and K are tied together.



(a) From JK flip-flop





The T flip-flop can be constructed with a D flip-flop and an exclusive-OR gates as shown in Fig. (b). The expression for the D input is

 $D = T \bigoplus Q = TQ` + T`Q$ 



(b) From D flip-flop

(c) Graphic symbol



**D** flip-flop Characteristic Equations

Q(t+1) = D

JK flip-flop Characteristic Equations

Q(t + 1) = JQ' + K'Q

T flip-flop Characteristic Equations

$$Q(t + 1) = T \bigoplus Q = TQ` + T`Q$$



Some flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state independent of the clock. The input that sets the flip-flop to 1 is called present or direct set. The input that clears the flip-flop to 0 is called clear or direct reset. When power is turned on a digital system, the state of the flip-flops is unknown. The direct inputs are useful for bringing all flip-flops in the system to a known starting state prior to the clocked operation.

### **D Flip-Flop with Asynchronous Reset**

A positive-edge-triggered D flip-flop with asynchronous reset is shown in Fig(a).



(a) Circuit diagram

#### **D Flip-Flop with Asynchronous Reset**



 $R \ C \ D \ Q \ Q'$ 0 X X 0 1 

(b) Function table

(b) Graphic symbol

#### **5-4 Analysis of Clocked Sequential Circuits**

The analysis of a sequential circuit consists of obtaining a table or a diagram for the time sequence of inputs, outputs, and internal states. It is also possible to write Boolean expressions that describe the behavior of the sequential circuit. These expressions must include the necessary time sequence, either directly or indirectly.



The behavior of a clocked sequential circuit can be described algebraically by means of state equations. A state equation specifies the next state as a function of the present state and inputs. Consider the sequential circuit shown in Fig. 5-15. It consists of two D flip-flops A and B, an input x and an output y.





A(t+1) = A(t) x(t) + B(t) x(t)

B(t+1) = A'(t) x(t)

A state equation is an algebraic expression that specifies the condition for a flip-flop state transition. The left side of the equation with (t+1) denotes the next state of the flipflop one clock edge later. The right side of the equation is Boolean expression that specifies the present state and input conditions that make the next state equal to 1.

Y(t) = (A(t) + B(t)) x(t)



The time sequence of inputs, outputs, and flip-flop states can be enumerated in a state table (sometimes called transition table).

Table 5-2      State Table for the Circuit of Fig. 5-15					5-15	Table 5-3 Second Form o	f the State	Table	top present	
Pre St	sent	Input	Ne	ate	Output	Present	Next	State	Outpu	ıt
A	B	x	A	B	y	State		Continue of		-
0	0	0	0	0	0	otened as 4001	<i>x</i> = 0	x = 1	x = 0	<b>x</b> =
0	0	1	0	1	0	AB	AB	AB	y	y
0	1	0	0	0	1		Tores .			
0	1	1	1	1	0	00	00	01	0	0
1	0	0	0	0	1	01	00	11	And I will	0
1	1	0	0	0	1	10	00	10	1	0
1	1	1	1	0	Ô	11	00	10	1	0



The information available in a state table can be represented graphically in the form of a state diagram. In this type of diagram, a state is represented by a circle, and the transitions between states are indicated by directed lines connecting the circles.

1/0 : means input =1 output=0



Fig. 5-16 State Diagram of the Circuit of Fig. 5-15

#### **Flip-Flop Input Equations**

The part of the combinational circuit that generates external outputs is descirbed algebraically by a set of Boolean functions called **output equations**. The part of the circuit that generates the inputs to flip-flops is described algebraically by a set of Boolean functions called flip-flop **input equations**. The sequential circuit of Fig. 5-15 consists of two D flip-flops A and B, an input x, and an output y. The logic diagram of the circuit can be expressed algebraically with two flip-flop input equations and an output equation:

$$D_A = Ax + Bx$$
$$D_B = A`x$$
$$y = (A + B)x`$$

#### **Analysis with D Flip-Flop**

The circuit we want to analyze is described by the input equation  $D_A = A \bigoplus x \bigoplus y$ 

The D<sub>A</sub> symbol implies a D flip-flop with output A. The x and y variables are the inputs to the circuit. No output equations are given, so the output is implied to come from the output of the flip-flop.



(a) Circuit diagram

## **Analysis with D Flip-Flop**

The binary numbers under Axy are listed from 000 through 111 as shown in Fig. 5-17(b). The next state values are obtained from the state equation  $A(t+1) = A \bigoplus x \bigoplus y$ 

The state diagram consists of two circles-one for each state as shown in Fig. 5-17(c)



#### **Analysis with JK Flip-Flops**



Fig. 5-18 Sequential Circuit with JK Flip-Flop

#### **Analysis with JK Flip-Flop**

The circuit can be specified by the flip-flop input equations

 $J_{A} = B \qquad K_{A} = Bx`$  $J_{B} = x` \qquad K_{B} = A`x + Ax` = A \bigoplus x$ 

Present State		Input	Next State		Flip-Flop Inputs			
A	В	x	A	В	JA	KA	JB	KB
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1 lish og	1	1	1	0
0	1000	a dia hara	1	0	1	0	0	1
1	0	0	1	1.1	0	0	1	1
1	0	1	1.	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

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#### **Analysis with JK Flip-Flops**

A(t + 1) = JA` + K`AB(t + 1) = JB` + K`B

Substituting the values of JA and KA from the input equations, we obtain the state equation for A:

A(t + 1) = BA' + (Bx')A = AB + AB' + AB

The state equation provides the bit values for the column under next state of A in the state table. Similarly, the state equation for flip-flop B can be derived from the characteristic equation by substituting the values of J<sub>B</sub> and K<sub>B</sub>:

 $B(t + 1) = x B' + (A \bigoplus x) B = B x' + ABx + A Bx'$ 

## **Analysis with JK Flip-Flops**

The state diagram of the sequential circuit is shown in Fig. 5-19.



Fig. 5-19 State Diagram of the Circuit of Fig. 5-18

#### **Analysis With T Flip-Flops**

#### Characteristic equation $Q(t + 1) = T \bigoplus Q = T Q + TQ$



(a) Circuit diagram

(b) State diagram

#### **Analysis With T Flip-Flops**

Consider the sequential circuit shown in Fig. 5-20. It has two flip-flops A and B, one input x, and one output y. It can be described algebraically by two input equations and an output equation: Use present state

 $T_{A} = Bx$  $T_{B} = x$ y = AB

A(t+1)=(Bx)'A+(Bx)A'=AB'+Ax'+A'Bx

B(t+1)=x⊕B

Present State		Input		ate	Output	
A	В	UTANT I	A	B	R NY	
0	0	0	0	0	0	
0	0	1	0	1	0	
0	1	0	0	1	0	
0	1		1	0	0	
1	0	0	1961	0	0	
1	0	as see 1 and all ci	1	1	0	
1	1	0	1	1	policipo	
1	1	1	0	0	1	

## Mealy and Moore Models (1)

- The most general model of a sequential circuit has inputs, outputs, and internal states. It is customary to distinguish between two models of sequential circuits:
  - the Mealy model and the Moore model
- They differ in the way the output is generated.
  - In the Mealy model, the output is a function of both the present state and input.
- In the Moore model, the output is a function of the present state only.

## Mealy and Moore Models (2)

When dealing with the two models, some books and other technical sources refer to a sequential circuit as a finite state machine abbreviated FSM.

- The Mealy model of a sequential circuit is referred to as a Mealy FSM or Mealy machine.
- The Moore model is refereed to as a Moore FSM or Moore machine.

### Sequential Circuit Analysis

## Design of a simple sequential circuitAnalysis of an existing circuit

## State machine synthesis

- Creation of state machine
- State machines are digital sequential circuits that transition through a series of states according to their design.
- For the creation of any such circuit always start with the problem definition or the circuit specification.

## **Problem Statement**

- Design a 2 bit up counter that has no preset state and continually cycles thought the 4 states.
- This can be defined by a table called a state table.

	Present State	Next State
•	00	01
	01	10
	10	11
	11	00

## A diagram representation

This form is termed a state diagram



## Sequential circuits

#### Basic form and elements





- Storage Elements –
  2 Flip-flops
- No inputs
- Current state is the output
- Combination logic generate the next state value.



## **Generating Next State**

Use K maps generated from State Table





#### Using D FF



## Sequential Circuit analysis

 The circuit to analyze

#### How to start?

 How about with the next state equations?



## **Next State Equations**

- For D<sub>A</sub> have an AND-OR set of gates to generate the input.
  - The upper AND gate has inputs X and A
  - The lower AND gate has inputs X and B

• So 
$$D_A = AX + BX$$

For D<sub>B</sub> have a single AND gate whose inputs are X and A'

• So 
$$D_B = A'X$$

## Also have an output Y

- The OR gate has inputs A and B
- This feeds into a 2-input AND gate whose other input is X'
- Thus Y = (A+B)X'
- Now having these equations can construct the state table for the state machine

## The state table

For generation of the next state you have the Present State as indicated by A and B plus the input X. This next state becomes the current state on the clock.

Present State		Input	Nex	t State	Output
A	в	x	A	в	Y
0	0	0	0	0	0
0	0	1	0	.1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

State Table for Circuit of Figure 5-15

# Another form of the state table

#### Two-dimensional form of the same table

#### TABLE 5-2

Two-Dimensional State Table for the Circuit in Figure 5-15

Present state		•	Next	state	Ð	Ou	tput
		X	<b>X</b> = 0		= 1	$\mathbf{x} = 0$	X = 1
A	в	A	в	A	в	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

## The state Diagram

- The state diagram for this systems is
- Not the notation on the diagram
  - On transition arcs
     input/output

